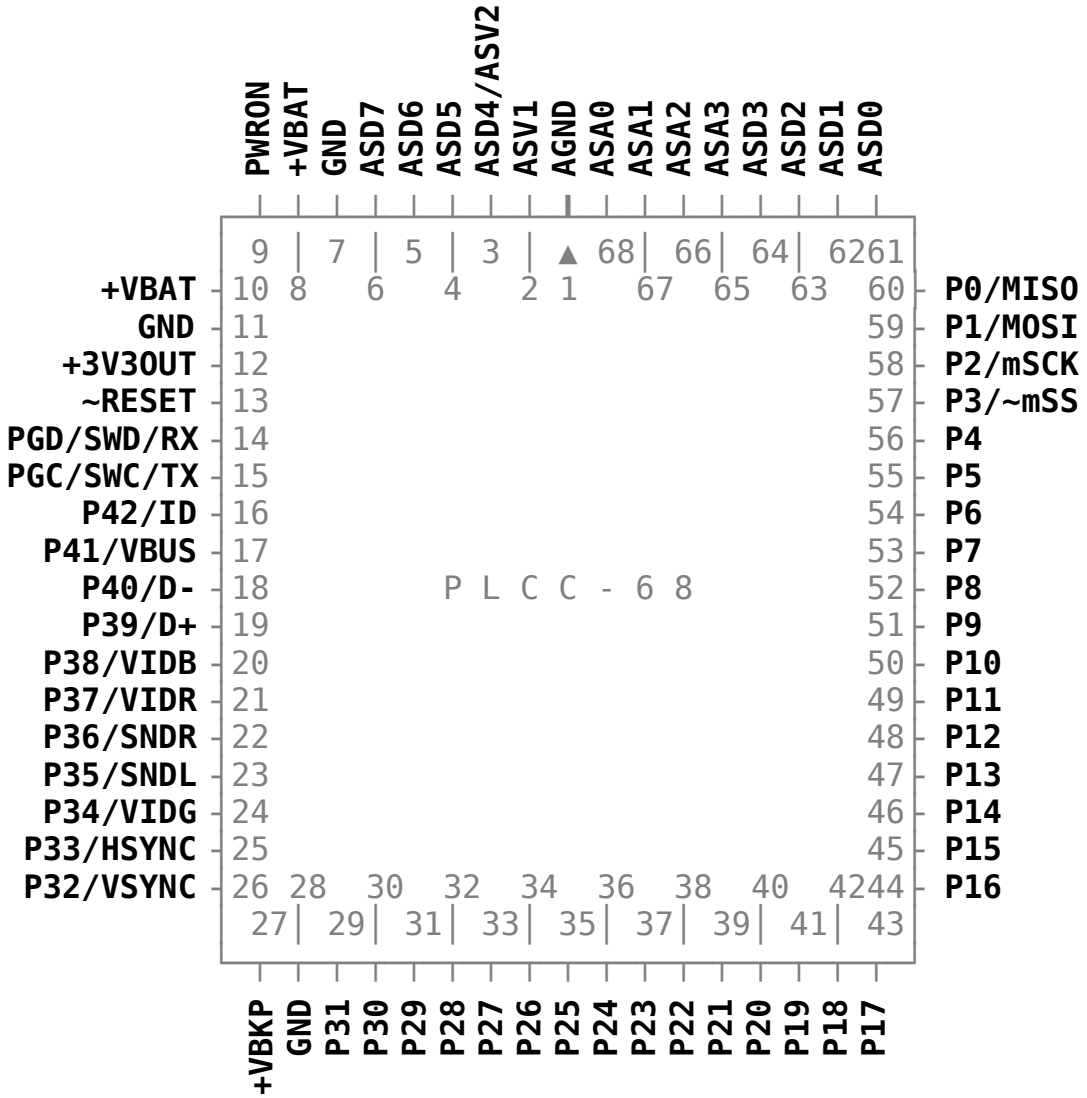
July 2013

Application Note 0003
DTX Bus Pinout

The embedded modules, members of the DTX series (2nd generation), use unified pinout model, based on the PLCC68 package format. The available 68 lines are assigned to various functions and modules use only those whose functionality are supported, leaving the rest unconnected. This model allows all the modules to be bus-wired without any mutually exclusive functions resulting unwanted situations.



1. Pinout Summary

All 2nd generation DTX modules should conform to this pinout and cover or exceed the specified input voltages and not exceed the specified output voltages, in order to ensure normal operation of the bus.

Pin	Name	Allowed Function	Voltage to (A)GND [V]	Description
1	AGND	P		Analogue or application specific Ground
2	ASV1	P	undefined	Application specific voltage 1 *(power/reference)*
3	ASD4/ASV2	P	undefined	Application specific with respect to GND/AGND *(preferred digital)* Application specific voltage 2 *(power/reference)*
4	ASD5	any	undefined	Application specific with respect to GND/AGND *(preferred digital)*
5	ASD6	any	undefined	Application specific with respect to GND/AGND *(preferred digital)*
6	ASD7	any	undefined	Application specific with respect to GND/AGND *(preferred digital)*
7	GND	P		Ground
8	+VBAT	P	-0.3 ... 18.0	Positive power lead
9	PWRON	I	-0.3 ... 18.0	Power enabling input (can be connected directly to +VBAT); active high
10	+VBAT	P	-0.3 ... 18.0	Positive power lead
11	GND	P		Ground
12	+3V3OUT	O,P	3.10 ... 3.45	+3.3V regulated output *(if available; output power varies)*
13	~RESET	I	-0.3 ... 9.0	General $\overline{\text{RESET}}$ input; active low
14	PGD/SWD/RX	I,O	-0.3 ... 5.5	Program/Debug data Serial Wire Debug *(Data)* UART RX input
15	PGC/SWC/TX	I,O	-0.3 ... 5.5	Program/Debug clock Serial Wire Debug *(Clock)* UART TX output
16	P42/ID	any	-0.3 ... 5.5	Any function within the specified voltage ID in USB OTG
17	P41/VBUS	any	-0.3 ... 5.5	Any function within the specified voltage USB Vbus power

18	P40/D-	any	-0.3 ... 5.5	Any function within the specified voltage USB D- line (host, device or OTG)
19	P39/D+	any	-0.3 ... 5.5	Any function within the specified voltage USB D+ line (host, device or OTG)
20	P38/VIDB	any	-1.2 ... 3.6	Any function within the specified voltage Video signal output (BLUE component)
21	P37/VIDR	any	-1.2 ... 3.6	Any function within the specified voltage Video signal output (RED component)
22	P36/SNDR	any	-1.2 ... 3.6	Any function within the specified voltage Sound channel output (RIGHT channel)
23	P35/SNDL	any	-1.2 ... 3.6	Any function within the specified voltage Sound channel output (LEFT channel)
24	P34/VIDG	any	-1.2 ... 3.6	Any function within the specified voltage Video signal output (GREEN component)
25	P33/HSYNC	any	-1.2 ... 3.6	Any function within the specified voltage Video signal horizontal synchronisation
26	P32/VSYNC	any	-1.2 ... 3.6	Any function within the specified voltage Video signal vertical synchronisation
27	+VBKP	P	-0.3 ... 3.8	Backup power supply; positive lead
28	GND	P		Ground
29	P31	any	-0.3 ... 3.6	Any function within the specified voltage
30	P30	any	-0.3 ... 3.6	Any function within the specified voltage
31	P29	any	-0.3 ... 3.6	Any function within the specified voltage
32	P28	any	-0.3 ... 3.6	Any function within the specified voltage
33	P27	any	-0.3 ... 3.6	Any function within the specified voltage
34	P26	any	-0.3 ... 3.6	Any function within the specified voltage
35	P25	any	-0.3 ... 3.6	Any function within the specified voltage
36	P24	any	-0.3 ... 3.6	Any function within the specified voltage
37	P23	any	-0.3 ... 3.6	Any function within the specified voltage
38	P22	any	-0.3 ... 3.6	Any function within the specified voltage
39	P21	any	-0.3 ... 3.6	Any function within the specified voltage
40	P20	any	-0.3 ... 3.6	Any function within the specified voltage
41	P19	any	-0.3 ... 3.6	Any function within the specified voltage
42	P18	any	-0.3 ... 3.6	Any function within the specified voltage
43	P17	any	-0.3 ... 3.6	Any function within the specified voltage
44	P16	any	-0.3 ... 3.6	Any function within the specified voltage
45	P15	any	-0.3 ... 3.6	Any function within the specified voltage

46	P14	any	-0.3 ... 3.6	Any function within the specified voltage
47	P13	any	-0.3 ... 3.6	Any function within the specified voltage
48	P12	any	-0.3 ... 3.6	Any function within the specified voltage
49	P11	any	-0.3 ... 3.6	Any function within the specified voltage
50	P10	any	-0.3 ... 3.6	Any function within the specified voltage
51	P9	any	-0.3 ... 3.6	Any function within the specified voltage
52	P8	any	-0.3 ... 3.6	Any function within the specified voltage
53	P7	any	-0.3 ... 5.5	Any function within the specified voltage
54	P6	any	-0.3 ... 5.5	Any function within the specified voltage
55	P5	any	-0.3 ... 5.5	Any function within the specified voltage
56	P4	any	-0.3 ... 5.5	Any function within the specified voltage
57	P3/~mSS	any	-0.3 ... 5.5	Any function within the specified voltage mSPI slave select *(default for slave devices only)*; active low
58	P2/mSCK	any	-0.3 ... 5.5	Any function within the specified voltage mSPI clock *(generated by the Master)*
59	P1/MOSI	any	-0.3 ... 5.5	Any function within the specified voltage mSPI Master-Out-Slave-In
60	P0/MISO	any	-0.3 ... 5.5	Any function within the specified voltage mSPI Master-In-Slave-Out
61	ASD0	any	undefined	Application specific with respect to GND/AGND *(preferred digital)*
62	ASD1	any	undefined	Application specific with respect to GND/AGND *(preferred digital)*
63	ASD2	any	undefined	Application specific with respect to GND/AGND *(preferred digital)*
64	ASD3	any	undefined	Application specific with respect to GND/AGND *(preferred digital)*
65	ASA3	any	undefined	Application specific with respect to AGND/GND *(preferred analogue)*
66	ASA2	any	undefined	Application specific with respect to AGND/GND *(preferred analogue)*
67	ASA1	any	undefined	Application specific with respect to AGND/GND *(preferred analogue)*
68	ASA0	any	undefined	Application specific with respect to AGND/GND *(preferred analogue)*

Legend:
I – input with CMOS level
P – power
O – digital output
OD – open drain output
AI – analogue input
AO – analogue output

2. General Recommendations

All application-specific lines and voltages should not be bus-wired among devices with unknown functionaity.

It is acceptable if a device only uses one +VBAT pin and one GND pin. In such case the pair pins 10 and 11 should given advantage.

If a device is acting both as mSPI master and slave roles, it is its responsibility to properly handle the dedicated mSPI lines according to its current role.

The +3V3OUT line can be bus-wired (although that is not recommended) and devices, which are outputing power on it should make sure the voltage on this output of theirs is strictly within the specified range.